REMARKS

Claims 1-17 are pending in this application, of which claims 11-17 have been withdrawn from consideration. Claims 18 and 19 have been canceled. Reconsideration of the rejections in view of these amendments and the following remarks is respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment, which is captioned "Version with Markings to Show Changes Made."

Rejections under 35 U.S.C. §103

Claims 1, 2, 5 and 6 stand rejected under 35 U.S.C. 103(a) as being unpatentable over K. Kasai et al. (*W/WNx/Poly-Si Gate Technology for Future High Speed Deep Submicron CMOS LSIs*) in view of Jeng et al. (U.S. Patent No. 5,877,074).

Applicants respectfully traverse this rejection.

Claims 1 and 2, have been amended to recite "a second polycrystalline silicon film formed on the first polycrystalline silicon film having a thickness of 2-20 nm and thinner than that of the first polycrystalline silicon film."

Claims 1, 2, 5 and 6 recite that the second polycrystalline silicon film has a thickness of 2-20 nm and thinner than that of the first polycrystalline silicon film. In the present invention, the second polycrystalline silicon film having crystal grain boundaries which are discontinuous to the first polycrystalline silicon film is formed between the first polycrystalline silicon film and the metal nitride film so as to prevent the dopant impurity (boron) in the first polycrystalline silicon film from being absorbed by the metal nitride

film. The diffusion of the dopant impurity in the first polycrystalline silicon film toward the metal nitride film is suppressed by the second polycrystalline silicon film. However, if the second polycrystalline silicon film is too thick, contact resistance between the first polycrystalline silicon film and the metal nitride film is increased. There is a risk that especially AC characteristics may be affected. Thus, the thickness of the second polycrystalline silicon film must be thinner than that of the first polycrystalline silicon film. It is preferable that the second polycrystalline silicon film is 2-20 nm-thick (see page 8, line 18 to page 9, line 10 of the specification of the present application).

In Kasai et al., in the step of forming the polycrystalline silicon layer of the gate electrode, a 100 nm-thick polycrystalline silicon film and a 100 nm-thick amorphous silicon film are sequentially deposited. However, FIG. 2 of Kasai et al. indicates that the final structure of the gate electrode to be formed by the above-described process has a 200 nm-thick single polycrystalline silicon layer. Kasai et al. merely discloses that the amorphous silicon film is formed in order to suppress impurity diffusion between n^+ and p^+ poly-Si during the fabrication process (see page 19.4.1, right column, lines 20-22). Kasai et al. neither teaches nor suggests the stack of the polycrystalline silicon films having thickness and grain boundary different from each other.

In Kasai et al., the amorphous silicon film is formed in order to suppress the interdiffusion of dopant impurities as described above. Thus, the thickness of the amorphous silicon film is set as 100nm, and the thickness ratio of the polycrystalline silicon film and the amorphous silicon film is set as 1: 1, respectively, in order to suppress interdiffusion of dopant impurities. Kasai et al. neither teaches nor suggests making the thickness of the amorphous silicon film thin.

Thus, Kasai et al. neither teaches nor suggests forming the polycrystalline silicon layer into a two-layer structure, and thinning the thickness of the upper polycrystalline silicon film to 2-20 nm.

The Examiner has alleged that Jeng et al. teaches in FIG. 5 a semiconductor device including: a gate electrode formed above the silicon substrate 11 with a gate insulation film 12 interposed therebetween, wherein the gate electrode is formed of a first polycrystalline silicon film 31 and a second polycrystalline silicon film 32 having a thickness thinner than that of the first polycrystal line silicon film 31. However, Jeng et al. relates to a semiconductor device having a so-called "polycide gate" structure in which the gate electrode is formed from a stack of the polycrystalline silicon film and the silicide film. On the other hand, both the present invention and Kasai et al. relate to a semiconductor device having a so-called "polymetal gate" structure in which the gate electrode is formed from a stack of the polycrystalline silicon film and the metal film. Thus, the basic gate structures of Jeng et al. are clearly different from that of the present invention and that of Kasai et al. With the polymetal gate structure and the polycide gate structure, the diffusion modes of impurities completely differ based on the difference in structures, e.g., whether or not a barrier metal layer is included, and the fabrication process. Thus, Jeng et al. is irrelevant to either the present invention or Kasai et al.

In Jeng et al., the amorphous silicon film 32 is formed between the polycrystalline silicon film 31 and the tungsten silicide film 14 in order to prevent the peeling of the tungsten silicide film 14 and the diffusion of the fluorine atoms introduced during the deposition of the tungsten silicide film 14 by CVD. Thus, the object of Jeng et al. also is different from that of the present invention and that of Kasai et al.

Thus, even though Jeng et al. discloses the 20-40 nm-thick polycrystalline silicon film 32, this disclosure does not teach or suggest using the 20-40 nm-thick polycrystalline silicon film in Kasai et al.

Thus, a person of ordinary skill in the art would not form the second polycrystalline silicon film of Kasai et al. to the thickness as taught by Jeng et al., even though Jeng et al. discloses that the gate electrode is formed of the first polycrystalline silicon film 31 and the second polycrystalline silicon film 32 having the thickness thinner than that of the first polycrystalline silicon film 31.

Thus, claims 1, 2, 5 and 6 patentably distinguish over Kasai et al. and Jeng et al., and the 35 U.S.C. §103(a) rejection should be withdrawn.

Claims 3, 4 and 7-10 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kasai et al. and Jeng et al., and further in view of Tsukamoto (U.S. 2001/0000629Al).

Applicants respectfully traverse this rejection.

The Examiner has alleged that Kasai et al. and Jeng et al. teach all the features of the claimed invention with the exception of explicitly disclosing an oxide film formed between tile first and second polycrystalline silicon films. The Examiner has also alleged that Tsukamoto teaches a native oxide film 20 is formed between the first 6 and second 7 polycrystalline silicon films so that the grain size of the second polycrystalline silicon film 7 can become large. Based on these disclosures, the Examiner has concluded that it would have been obvious to a person of ordinary skill in the art at the time of invention to form an oxide film between the first and second polycrystalline silicon films of Kasai et al. as taught by Tsukamoto to suppress fluctuation in the threshold voltage V th.

However, the alleged teaching of Tsukamoto does not remedy the deficiencies of Kasai et al. and Jeng et al. As discussed above, Kasai et al. and Jeng et al. are clearly different from the present invention and do not provide any motivation for the present invention. Thus, Claims 3, 4 and 7-10 patentably distinguish over the combination of Kasai et al., Jeng et al. and Tsukamoto., and the 35 U.S.C. §103(a) rejection should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, claims 1-10, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosures: Version with Markings to Show Changes Made
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VERSION WITH MARKINGS TO SHOW CHANGES MADE S.N. 09/749,590

IN THE CLAIMS:

Claims 18 and 19 have been canceled.

Claims 1-4 have been amended as follows:

1. (Twice Amended) A semiconductor device comprising:

a pair of impurity diffused regions formed in a silicon substrate, spaced from each other; and

a gate electrode formed above the silicon substrate between the pair of impurity diffused regions with a gate insulation film interposed therebetween, the gate electrode being formed of a first polycrystalline silicon film formed on the gate insulation film, a second polycrystalline silicon film formed on the first polycrystalline silicon film having a thickness of 2-20 nm and thinner than that of the first polycrystalline silicon film and having crystal grain boundaries which are discontinuous to the first polycrystalline silicon film, and a metal nitride film formed on the second polycrystalline silicon film.

2. (Twice Amended) A semiconductor device comprising:

a pair of impurity diffused regions formed in a silicon substrate, spaced from each other; and

a gate electrode formed above the silicon substrate between the pair of impurity diffused regions with a gate insulation film interposed therebetween, the gate electrode being formed of a first polycrystalline silicon film formed on the gate insulation film, a second polycrystalline silicon film formed on the first polycrystalline silicon film having a thickness of 2-20 nm and thinner than that of the first polycrystalline

silicon film and having crystal grain boundaries which are discontinuous to the first polycrystalline silicon film, a metal nitride film formed on the second polycrystalline silicon film, and a metal film form on the metal nitride film.

3. (Amended) A semiconductor device according to claim 1, wherein

a native oxide film or a chemical oxide film formed by liquid chemical treatment is formed between the first polycrystalline silicon film and the second polycrystalline silicon film.

4. (Amended) A semiconductor device according to claim 2, wherein

a native oxide film or a chemical oxide film formed by liquid chemical treatment is formed between the first polycrystalline silicon film and the second polycrystalline silicon film.